



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,063	02/20/2004	Tobias Scholand	5123-189US	6764

7590 04/16/2007
Richard C. Woodbridge, Esq.
Synnestvedt Lechner & Woodbridge, LLP
P.O. Box 592
Princeton, NJ 08542-0592

EXAMINER

MATIN, NURUL M

ART UNIT	PAPER NUMBER
----------	--------------

2611

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/783,063

Applicant(s)

SCHOLAND ET AL.

Examiner

Nurul M. Matin

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☒ Claim(s) 1 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 05/24/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:
In Page 2, Para [0028], line 4, a quadrature-phased base-band signal 16, it should be 18.
Appropriate correction is required.

Claim Objections

2. Claim 1 objected to because of the following informalities:
In claim 1, line 4 says, "bandlinimted" it should be bandlimited
Line 5 says, "frequenc" it should be frequency,
Line 6 says, "mulitplier" it should be multiplier.
Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-3, 8, 15 are rejected under 35 U.S.C. 102(b) as being unpatentable over Takeda et al, US 4551846 and in view of Friedmann et al, US 6223053.

Re claim 1, Takeda discloses a receiver for modulated incoming signals with a carrier frequency $f_{sub.0}$ and a bandwidth B , whereby a band-pass filter is limiting the incoming signal (fig.3, line 10-14, "A band pass filter 2 selects only the modulating frequency band of the FSK signal, and the signal is then limited in amplitude by a limiter 3"), characterized by the fact, that the "Zero-Crossing"-Decoder is part of a Microprocessor, and that the signal $s(t)$ is the input signal to one of the microprocessors inputs (E), whereby the microprocessor has a timer (or counter) which counts with a frequency $f_{sub.CL}$, whereby $f_{sub.CL}$ is smaller than the intermediate frequency $f_{sub.IF}$, and the microprocessor is determining (calculating) the time distances $\Delta_{sub.n}$ of the zero-crossings of the input signal using the timer (counter) values (col.1, line 39-46, " a plurality of counters are used for counting during a plurality of successive intervals between successive zero-cross points. The number of successive zero-cross points which are counted in each counter equals the number of counters which are used. Thus, at each zero-cross point another counter of the plurality of counters commences its count"). But Takeda fails to teach that a downstream multiplier is multiplying the bandlimited signal with a sinusoidal signal with a frequency $f < f_{sub.0}$, whereafter the output signal of the multiplier $s(t)$ is the input signal of a downstream "Zero-Crossing"-Decoder, whereby the output signal has an intermediate frequency $f_{sub.IF} = f_{sub.0} - f$, with $f_{sub.IF} > B/2$. However, Friedmann does (col.9, line 21-34, "The RF downconverter circuit 65 is driven by the same adjustable synthesizer 60 so as to mix down the received signal by applying the same selected fixed frequency or frequency hopping sequence. The RF downconverter circuit 65 mixes the received

signal down to a lower frequency and outputs the mixed down signal via line 108 to an adjustable demodulator 67").

Therefore, taking the combined teaching of Takeda and Friedmann, as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of a downstream multiplier is multiplying the bandlimited signal with a sinusoidal signal with a frequency $f < f_{sub.0}$, whereafter the output signal of the multiplier $s(t)$ is the input signal of a downstream "Zero-Crossing"-Decoder, whereby the output signal has an intermediate frequency $f_{sub.IF} = f_{sub.0} - f$, with $f_{sub.IF} > B/2$ as thought in Friedmann into Takeda so that the adjustable demodulator can carry out what is referred to as sinusoidal phase modulation (SPM) demodulation.

Re claim 2, Takeda and Friedmann references teach a Receiver according to claim 1, and Takeda reference also teaches a memory hold the values of the time intervals $\Delta_{sub.n}$ of one burst (col.8, line 56-59).

Re claim 3, Takeda and Friedmann references teach a Receiver according to claim 1 and Takeda reference also teaches a memory holds the values--as a vector e --of the time intervals $\Delta_{sub.n}$ each subtracted by the value $1/f_{sub.IF}$ (col.9, line 50-66).

Re claim 8, Takeda and Friedmann references teach a Receiver according to claim 1 and Takeda reference also teaches the frequency $f_{sub.CL}$ is within the parameters of $f_{sub.IF}/8 \leq f_{sub.CL} < f_{sub.\mu.Proc}$, with $f_{sub.\mu.Proc}$ is the frequency of the microprocessor or the timer (counter) (col.1, line 45-50).

Re claim 15, which claim the same subject matter as recited in claim 1.

Art Unit: 2611

Therefore, claim 15 has been analyzed and rejected with respect to claim 1.

2. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al, US 4551846, Friedmann et al, US 6223053 and in view of Kim et al, US 20040141480.

Re claim 4, Takeda and Friedmann fail to teach an estimator (decoder) is estimating the transmitted data by using an approximated linear system model ($e=Ad+n$) of the transmitting system. However, Kim does (page2, Para [0027], line 1-5).

Therefore, taking the combined teaching of Takeda, Friedmann and Kim, as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of an estimator (decoder) is estimating the transmitted data by using an approximated linear system model ($e=Ad+n$) of the transmitting system as thought in Kim into Takeda and Friedmann to modeled the solution of the communication signals.

Re claim 6, Takeda, Friedmann and Kim reference teach a receiver according to claim 4 or 5, and Kim reference also teaches the estimator is a linear filter, whereby a threshold device is applied to the output of the estimator for detecting the data values (abstract & also page 2, Para [0027], line 1-5).

3. Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al, US 4551846, Friedmann et al, US 6223053, Kim et al, US 20040141480 and in view of Olofsson et al, US 6167031.

Re claim 5, Takeda, Friedmann and Kim fail to teach that the estimator calculates the quality of each received data value, whereby the quality is a statement of the probability whether a transmitted data value was correctly transmitted. However, Olofsson does (col.4, line 60-65).

Therefore, taking the combined teaching of Takeda, Friedmann, Kim and Olofsson as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of the estimator calculates the quality of each received data value, whereby the quality is a statement of the probability whether a transmitted data value was correctly transmitted as thought in Olofsson into Takeda, Friedmann and Kim to provide the best user quality.

Re claim 7, Receiver according to claim 4 or 5, wherein the estimator is a Max-Log-ML detector (one of the ordinary skill in the art will know that the estimator is a Max-Log-ML detector which can be used in Bluetooth or DECT receivers).

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al, US 4551846, Friedmann et al, US 6223053 and in view of Turner et al, US 6646845.

Re claim 9, Takeda and Friedmann fail to disclose the input (E) of the microprocessor is a Timer input, counter input or a normal signal input. However, Turner does (col. 7, line 1-3).

Therefore, taking the combined teaching of Takeda, Friedmann and Turner, as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of the input (E) of the microprocessor is a Timer input, counter input or a

normal signal input as thought in Turner into Takeda and Friedmann to provides time data to the microprocessor.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al, US 4551846, Friedmann et al, US 6223053, Turner et al, US 6646845 and in view of Hirschmann et al, US 5990633.

Re claim 10, Takeda, Friedmann and Turner fail to teach a capacitor is in downstream of the multiplier. However, Hirschmann does (col.2, line 45-49).

Therefore, taking the combined teaching of Takeda, Friedmann, Turner and Hirschmann, as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of the a capacitor is in downstream of the multiplier as thought in Hirschmann into Takeda, Friedmann and Turner to provide the transfer energy required for a reliable transmission.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al, US 4551846, Friedmann et al, US 6223053, Turner et al, US 6646845 and in view of Kojima et al, US 5224643.

Re claim 11, Takeda, Friedmann and Turner fail to teach the signal $s(t)$ is free of direct voltage and that an Offset is added by an adder. However, Kojima does (col.9, line 60-63).

Therefore, taking the combined teaching of Takeda, Friedmann, Turner and Kojima, as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of the signal $s(t)$ is free of direct voltage and that an Offset

is added by an adder as thought in Kojima into Takeda, Friedmann and Turner so the phase control process can well be carried out immediately at any temperatures.

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al, US 4551846, Friedmann et al, US 6223053, Turner et al, US 6646845 and in view of Hiramatsu et al, US 5031191.

Re claim 12, Takeda, Friedmann and Turner reference fail to teach the receiver comprises more than one band-pass filters and multipliers for receiving multiple incoming signals with different frequencies $f_{sub.i,0}$, whereby a selector is selectively connecting the signals $s_{sub.i}(t)$ to the input of the microprocessor. However, Hiramatsu does (col.5, line 50-65 & col.20, line 46-68).

Therefore, taking the combined teaching of Takeda, Friedmann, Turner and Hiramatsu, as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of the receiver comprises more than one band-pass filters and multipliers for receiving multiple incoming signals with different frequencies $f_{sub.i,0}$, whereby a selector is selectively connecting the signals $s_{sub.i}(t)$ to the input of the microprocessor as thought in Hiramatsu into Takeda, Friedmann and Turner to provide a spread spectrum signal demodulation circuit in which a circuit configuration can be made simple(summary of the invention).

Re claim 13, Takeda, Friedmann, Turner and Hiramatsu references teach Receiver according to claim 9, and Hiramatsu reference also teaches the receiver comprises more than one band-pass filters and multipliers for receiving multiple

Art Unit: 2611

incoming signals with different frequencies $f_{sub,i}$, whereby each signal $s_{sub,i}(t)$ is the input signal for an input $E_{sub,i}$ of the microprocessor(col.5, line 50-65 & col.20, line 46-68).

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al, US 4551846, Friedmann et al, US 6223053 and in view of Kurakami et al, US 2003/0223510.

Re claim 14, Takeda and Friedmann fail to teach the incoming signal is a phase modulated signal, especially modulated with CPM (continuous phase modulation), especially a GSM, Bluetooth or DGPS-signal. However, Kurakami does (page 1, Para [0007], line 1-3).

Therefore, taking the combined teaching of Takeda, Friedmann and Kurakami, as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of the incoming signal is a phase modulated signal, especially modulated with CPM (continuous phase modulation), especially a GSM, Bluetooth or DGPS-signal as thought in Kurakami into Takeda and Friedmann so that a high frequency power amplification circuit at a final stage can be operated in a saturation region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nurul M. Matin whose telephone number is 571-270-1188. The examiner can normally be reached on mon-fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nurul Matin


MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER